1. A transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a conductive spacer formed around said gate structure on said secondary oxide layer, said conductive spacer including an aperture over a portion of said gate structure;

a first contact to said gate structure by way of said aperture; and

a second contact to said conductive spacer.

2. A dual gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a conductive spacer formed around said gate structure on said secondary oxide layer, said conductive spacer defining a second gate and including an aperture over a portion of said gate structure;

a first contact to a portion of said gate structure corresponding to said aperture; and

a second contact to said conductive spacer.

3. A transistor structure comprising:

an actual gate and a pseudo gate formed on a first oxide layer on a semiconductor structure, said actual and pseudo gates being separated from one another;

a secondary oxide layer formed over said actual and pseudo gates;

a conductive spacer formed around said actual and pseudo gates on said secondary oxide layer, said conductive spacer including an aperture over a portion of said actual gate;

a first contact to a portion of said actual gate corresponding to said aperture; and

a second contact to said conductive spacer at said pseudo gate.

4. A method of making a transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure;

forming a secondary oxide layer on said gate structure;

forming a conductive spacer around said gate structure on said secondary oxide layer;

removing said conductive spacer from a portion of said gate structure;

forming a first contact to said portion of said gate structure from which said conductive spacer has been removed; and

forming a second contact to said conductive spacer.

5. A method of making a transistor structure comprising the steps of:

forming a gate on a first oxide layer on a semiconductor structure;

forming a conductive spacer connection support on said first oxide layer on said semiconductor structure but separated from said gate;

forming a secondary oxide layer on said gate and said conductive spacer connection support;

forming a conductive spacer on said gate and said conductive spacer connection support on said secondary oxide layer;

removing said conductive spacer from a portion of said gate;

forming a first contact to said portion of said gate structure from which said conductive spacer has been removed; and

forming a second contact to said conductive spacer at said conductive spacer connection support.

6. A method of making a dual gate transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure to define a first gate;

forming a secondary oxide layer over said gate structure;

forming a conductive spacer around said gate structure on said secondary oxide layer to define a second gate;

removing said conductive spacer from a portion of said gate structure;

forming a first contact to said first gate at said portion of said gate structure from which said conductive spacer has been removed; and

forming a second contact to said conductive spacer.

7. A method of making a transistor structure comprising the steps of:

forming an actual gate on a first oxide layer on a semiconductor structure;

forming a pseudo gate on said first oxide layer on said semiconductor structure;

forming a secondary oxide layer over said actual gate and said pseudo gate;

forming a conductive spacer on said actual gate and said pseudo gate on said secondary oxide layer;

removing said conductive spacer from a portion of said actual gate;

forming a first contact to said actual gate at said portion of said actual gate from which said conductive spacer has been removed; and

forming a second contact to said conductive spacer at said pseudo gate.

8. An integrated circuit structure comprising:

a first plurality of conventional LDD transistors; and

a second plurality of transistors each comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a conductive spacer formed around said gate structure on said secondary oxide layer, said conductive spacer including an aperture over a portion of said gate structure;

a first contact to said gate structure at a portion of said gate structure corresponding to said aperture; and

a second contact to said conductive spacer, said first plurality of conventional LDD transistors and said second plurality of transistors being interconnected to form said integrated circuit structure.

9. An integrated circuit structure as claimed in claim 8 wherein said integrated circuit structure includes output drivers comprising at least a portion of said second plurality of transistors.

10. A method of making an integrated circuit structure comprising the steps of:

forming gate structures on a first oxide layer on a semiconductor structure;

forming a secondary oxide layer on said gate structures;

forming conductive spacers around said gate structures;

utilizing said conductive spacers to form LDD transistor structures associated with a first number of said gate structures;

utilizing said conductive spacers to form transistor structures associated with a second number of said gate structures by performing the steps of:

removing said conductive spacer from portions of said second number of said gate structures;

forming first contacts to said second number of gate structures at said portions of said second number of gate structures from which said conductive spacer has been removed; and

forming second contacts to said conductive spacers.

11. A transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a conductive layer formed around said gate structure on said secondary oxide layer, said conductive layer including an aperture over a portion of said gate structure;

a nonconductive spacer formed over said conductive layer, said nonconductive spacer including an aperture at least partially aligned with said aperture through said conductive layer;

a first contact to said gate structure at a portion of said gate structure corresponding to said apertures; and

a second contact to said conductive layer.

12. A dual gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a conductive layer formed on said secondary oxide on said gate structure, said conductive layer defining a second gate and including an aperture over a portion of said gate structure;

a nonconductive spacer formed over said conductive layer, said nonconductive spacer including an aperture at least partially aligned with said aperture through said conductive layer;

a first contact to said first gate at a portion of said gate structure corresponding to said apertures; and

a second contact to said conductive layer.

13. A transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a conductive layer formed on said secondary oxide layer on said gate structure, said conductive layer including an aperture over a portion of said gate structure and forming a first conductive portion of a spacer;

a nonconductive layer formed over said conductive layer, said nonconductive spacer including an aperture at least partially aligned with said aperture through said conductive layer and forming a second nonconductive portion of said spacer;

a first contact to said gate structure at a portion of said gate structure corresponding to said apertures; and

a second contact to said conductive layer.

14. A transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a composite spacer formed on said secondary oxide layer on said gate structure, said composite spacer comprising a conductive layer formed over said gate structure and a nonconductive layer formed over said conductive layer, said composite spacer including an aperture over a portion of said gate structure;

a first contact to said gate structure by way of a portion of said gate structure corresponding to said aperture; and

a second contact to said conductive layer of said composite spacer.

15. A multiple gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer.

16. A multiple gate transistor as claimed in claim 15 wherein said spacer is formed on a first side of said gate structure to form a second gate and a second side of said gate structure to form a third gate, said second contact being to said conductive portion of said spacer defining said second gate and said multiple gate transistor further comprising a third contact to said conductive portion of said spacer defining said third gate.

17. A two gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a first contact to said gate structure; and

a second contact to said conductive portion of said first portion of said spacer.

18. A three gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a second portion of said spacer formed on a second side of said gate structure on said secondary oxide layer, at least a portion of said second portion of said spacer adjacent to said secondary oxide layer being conductive and defining a third gate;

a first contact to said gate structure;

a second contact to said conductive portion of said first portion of said spacer; and

a third contact to said conductive portion of said second portion of said spacer.

19. An integrated circuit structure comprising:

a first plurality of conventional transistors; and

a second plurality of transistors each comprising:

a gate structure formed on a first oxide layer on a semiconductor structure;

a secondary oxide layer formed on said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer, said first plurality of conventional transistors and said second plurality of transistors being interconnected to form said integrated circuit structure.

20. An integrated circuit structure as claimed in claim 19 further comprising a third plurality of conventional LDD transistors, said third plurality of conventional LDD

transistors being interconnected to said first plurality of said conventional transistors to form said integrated circuit structure.

21. An integrated circuit structure as claimed in claim 20 wherein said third plurality of conventional LDD transistors are interconnected to said second plurality of transistors to form said integrated circuit structure.

22. An integrated circuit structure as claimed in claim 19 further comprising a third plurality of conventional LDD transistors, said third plurality of conventional LDD transistors being interconnected to said second plurality of transistors to form said integrated circuit structure.

23. A transistor structure comprising:

an actual gate and a pseudo gate formed on a first oxide layer on a semiconductor structure, said actual and pseudo gates being separated from one another;

a secondary oxide layer formed over said actual and pseudo gates;

a spacer formed on at least one side of said actual gate and on said pseudo gate on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said actual gate; and

a second contact to said conductive portion of said spacer at said pseudo gate.

24. A method of making a transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure;

forming a secondary oxide layer on said gate structure;

forming a conductive layer around said gate structure on said secondary oxide layer;

forming a nonconductive spacer over said conductive layer;

removing said conductive layer and said nonconductive spacer from a portion of said gate structure;

forming a first contact to said portion of said gate structure from which said conductive layer and nonconductive spacer have been removed; and

forming a second contact to said conductive layer.

25. A method of making a transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure;

forming a connection support on said first oxide layer on said semiconductor structure but separated from said gate structure;

forming a secondary oxide layer on said gate structure and said connection support;

forming a conductive layer around said gate structure and said connection support on said secondary oxide layer;

forming a nonconductive spacer over said conductive layer;

removing said nonconductive spacer from a portion of said gate structure;

removing said conductive layer from said portion of said gate structure;

forming a first contact to said portion of said gate structure from which said nonconductive spacer and said conductive layer have been removed; and

forming a second contact to said conductive layer at said connection support.

26. A method of making a transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure;

forming a secondary oxide layer on said gate structure;

forming a composite spacer around said gate structure on said secondary oxide layer, said composite spacer comprising a conductive layer formed over said gate structure and a nonconductive layer formed over said conductive layer;

removing said composite spacer from a portion of said gate structure;

forming a first contact to said portion of said gate structure from which said composite spacer has been removed; and

forming a second contact to said conductive layer of said composite spacer.

27. A method of making a multiple gate transistor structure comprising the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure to define a first gate;

forming a secondary oxide layer over said gate structure;

forming a spacer on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

forming a first contact to said gate structure; and

forming at least a second contact to said conductive portion of said spacer.

28. A method for making a multiple gate transistor as claimed in claim 27 wherein said step of forming a spacer comprises the steps of:

forming a spacer on a first side of said gate structure to form a second gate;

forming a spacer on a second side of said gate structure to form a third gate separate from said second gate;

forming said second contact to said conductive portion of said spacer defining said second gate; and

said method further comprising the step of forming a third contact to said conductive portion of said spacer defining said third gate.

29. A method of making an integrated circuit structure comprising the steps of:

forming a first plurality of conventional transistors; and

forming a second plurality of transistors by performing the steps of:

forming a gate structure on a first oxide layer on a semiconductor structure;

forming a secondary oxide layer on said gate structure;

forming a spacer on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

forming a first contact to said gate structure;

forming at least a second contact to said conductive portion of said spacer; and

interconnecting said first plurality of conventional transistors and said second plurality of transistors to form said integrated circuit structure.

30. A method of making an integrated circuit structure as claimed in claim 29 further comprising the steps of:

forming a third plurality of conventional LDD transistors, and

interconnecting said third plurality of conventional LDD transistors to said first plurality of said conventional transistors to form said integrated circuit structure.

31. A method of making an integrated circuit structure as claimed in claim 30 further comprising the step of interconnecting said third plurality of conventional LDD transistors to said second plurality of transistors to form said integrated circuit structure.

32. A method of making an integrated circuit structure as claimed in claim 29 further comprising the steps of:

forming a third plurality of conventional LDD transistors, and

interconnecting said third plurality of conventional LDD transistors to said second plurality of transistors to form said integrated circuit structure.